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EXAMINER	
GEBRIEL, SELAM T	

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2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/662,445	AGAN, MARTIN J.	
	Examiner	Art Unit	
	SELAM T. GEBRIEL	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-106* is/are pending in the application.

4a) Of the above claim(s) *4,13,24-26,40,54-56,65,67,68,77,79-81,91,98,100-102* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12,14-23,27-39,41-53,57-64,66,69-76,78,82-90,92-97,99 and 103-106* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1-3,5-12,14-23,27-39,41-53,57-64,66,69-76,78,82-90,92-97,99 and 103-106.

DETAILED ACTION

Response to Election of species requirement

1. Applicant's election without traverse of the Species 1, directed to Figure 3 and claims 1 – 3, 5 – 12, 14 – 23, 27 – 39, 41 – 53, 57 – 64, 66, 69 – 76, 78, 82 – 90, 92 – 97, 99 and 103 – 106 for continued examination in the reply filed on 09/29/2008 is acknowledged.

2. Claims 4, 13, 24 – 26, 40, 54 – 56, 65, 67, 68, 77, 79 – 81, 91, 98, and 100 – 102 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species. Election was made **without** traverse in the reply filed on 07/29/2008.

Claim Objections

3. Claim 2 is objected to the following informalities "Said photosensor" lack antecedent basis.

4. Claim 69 is objected to the following informalities "Said at least two reset transistors" lack antecedent basis.

Appropriate correction is needed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 – 3, 5 – 9, 11, 12, 14 – 16, 31 – 39, 41 – 49, 51 – 53, 57, 59 – 64, 66, 69 – 76, 78, 82 – 90, 92 – 97, 99, 103 – 106 are rejected under 35 U.S.C. 102(b) as being anticipated by Compton (US 2004/0081446 A1).

7. Regarding claim 1, Compton discloses a method of operating a pixel sensor cell (Figure 1, Element 10) of an image sensor (Figure 2, Element 90) comprising:

Opening a mechanical shutter (Page 2, Section 0016 and 0019, See Figure 5A – 5D);

Resetting a photoconversion device (Figure 1, Element 20) to begin an integration period after said shutter is opened (Page 2, Section 0016 and 0019 See Figure 5A – 5D);

Accumulating photo generated charge in said photoconversion device during said integration period (Page 2, Section 0016 and 0019, See Figure 5A – 5D);

Closing said shutter to end said first integration period (Page 2, Section 0016 and 0019, and 0020, See Figure 5A – 5D).

8. Regarding claim 2, Compton discloses a method as in claim 1 wherein said act of resetting said photosensor comprises coupling said photoconversion device to a voltage source (Page 2, Section 0016 and 0019, and 0020).

9. Regarding claim 3, Compton discloses a method as in claim 2 wherein said photoconversion device is coupled to a voltage source through a reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

10. Regarding claim 4, Compton discloses a method as in claim 3 wherein said photoconversion device is coupled to said voltage source directly by said reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

11. Regarding claim 5, Compton discloses a method as in claim 3 wherein said photoconversion device is coupled to said voltage source through said reset transistor and a transfer transistor which transfers accumulated charge from said photoconversion device (Page 2, Section 0015 – 0016, See figure 1, VDD and Photodiode 20 are connected through the reset gate 80 and transfer gate 30).

12. Regarding claim 6, Compton discloses a method of operating a pixel sensor cell of an image sensor comprising:

Opening a mechanical shutter (Page 2, Section 0016 and 0019, See Figure 5A – 5D);

Resetting a photoconversion device after said mechanical shutter is opened to begin a first integration period (Page 2, Section 0016 and 0019 See Figure 5A – 5D);

Accumulating charge in said photoconversion device during said first integration period (Page 2, Section 0016 and 0019, See Figure 5A – 5D);

Resetting a charge collection region (Floating Diffusion 40) and obtaining a reset voltage (Page 2 Section 0015);

Transferring said charge from said photoconversion device to said charge collection region (Page 2, Section 0015); and

Reading out the charge residing in said charge collection region to obtain a pixel signal voltage (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

13. Regarding claim 7, Compton discloses the method of claim 6, wherein said pixel sensor cell comprises:

A reset transistor (A reset gate 50) for resetting said charge collection region (Page 2, Section 0015, the charge collection region or the floating region is reset by a reset gate 50) and

A transfer transistor for transferring charge to said charge collection region (Page 2, Section 0015) and

Wherein said photoconversion device resetting comprises turning on said reset transistor and said transfer transistor (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

14. Regarding claim 8, Compton discloses the method of claim 7, wherein said reset transistor and said transfer transistor are turned on simultaneously (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

15. Regarding claim 9, Compton discloses the method of claim 7, wherein said pixel sensor cell further comprises reading out said charge through an output transistor and a row selection transistor (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select

transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

16. Regarding claim 11, Compton discloses the method of claim 6, wherein said photoconversion resetting comprises coupling said photoconversion device to a voltage source (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

17. Regarding claim 12, Compton discloses a method as in claim 11, wherein said photoconversion device is coupled to a voltage source through a reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

18. Regarding claim 13, Compton discloses a method as in claim 12, wherein said photoconversion device is coupled to said voltage source directly by said reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

19. Regarding claim 14, Compton discloses a method as in claim 12, wherein said photoconversion device is coupled to said voltage source through said reset transistor and a transfer transistor which transfers accumulated charge from said photoconversion device (Page 2, Section 0015 – 0016, See figure 1, VDD and Photodiode 20 are connected through the reset gate 80 and transfer gate 30).

20. Regarding claim 15, Compton discloses the method of claim 6, wherein said image sensor is a CMOS image sensor (See Page 1, Section 0001 and Sections 0002 – 0005 to see how this limitation is met, It talks about image sensors having reset synchronized with mechanical shutter for controlling exposure).

21. Regarding claim 16, Compton discloses the method of claim 6, wherein said charge collection region (Floating Diffusion 40) is a floating diffusion region (Page 1, Section 0015, and the charge collection region is Floating Diffusion 40).

22. Regarding claim 31, Compton discloses a method of operating a plurality of pixels in an array of an image sensor comprising:

Opening a mechanical shutter (Page 2, Section 0016 and 0019, See Figure 5A – 5D);

Globally resetting the pixels to begin a first integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20);

Accumulating charge in at least one photoconversion device of each pixel (Page 2, Section 0015);

Closing said shutter to end said first integration period (Page 2, Section 0016 and 0019, and 0020, See Figure 5A – 5D);

Resetting the pixels to obtain a respective reset voltage for each pixel and reading out said reset voltage (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing);

Transferring accumulated charge from each photoconversion device to an associated charge collection region of each pixel (Page 2, Section 0015 and 0016); and

Reading out the charge residing in each charge collection region to obtain a respective signal voltage for each pixel (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

23. Regarding claim 32, Compton discloses the method of claim 31, wherein the reset and signal voltages of said pixels are readout on a row by row basis after the mechanical shutter is closed and the first integration period ends (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for

passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

24. Regarding claim 33, Compton discloses the method of claim 31, wherein said global reset is conducted by turning on a reset transistor and a transfer transistor within each pixel to couple the photo conversion device of each pixel to a voltage source (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

25. Regarding claim 34, Compton discloses the method of claim 33, wherein said reset transistor and said transfer transistor are turned on simultaneously to begin said integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

26. Regarding claim 35, Compton discloses the method of claim 31, wherein said global reset is conducted by turning on a reset transistor in each pixel for resetting a photoconversion device (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

27. Regarding claim 36, Compton discloses the method of claim 31, wherein said image sensor is a CMOS image sensor (See Page 1, Section 0001 and Sections 0002 – 0005 to see how this limitation is met, It talks about image sensors having reset synchronized with mechanical shutter for controlling exposure).

28. Regarding claim 37, Compton discloses the method of claim 31, wherein said charge collection region is a floating diffusion region (Page 1, Section 0015, and the charge collection region is Floating Diffusion 40).

29. Regarding claim 38, Compton discloses the method of claim 37, wherein said act of reading out the reset voltage comprises reading out the reset voltage from said floating diffusion region (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

30. Regarding claim 39, Compton discloses the method of claim 31, wherein said pixel comprises four transistors (See Figure 1).

31. Regarding claim 41, Compton discloses a pixel sensor cell (Figure 3) comprising:

A photoconversion device (Figure 1, Element 20, Page 2, Section 0015) for accumulating charge;

A reset transistor and a transfer transistor for resetting said photoconversion device to begin an integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20);

A mechanical shutter, wherein said mechanical shutter is open during the resetting of said photoconversion device and closed to end said integration period (Page 2, Section 0016 and 0019, See Figure 5A – 5D);

A charge collection region for receiving said charge from said photoconversion device (Page 2, Section 0015, the charge collection region or the floating region is reset by a reset gate 50 and receives charge from the photoconversion device); and

A readout circuit (Figure 1, Element 150) for reading out said charge from said charge collection region (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

32. Regarding claim 42, Compton discloses the pixel sensor cell of claim 41, wherein said photoconversion device is coupled to a voltage source (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

33. Regarding claim 43, Compton discloses the pixel sensor cell of claim 42, wherein said photoconversion device is coupled to a voltage source through a reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

34. Regarding claim 44, Compton discloses the pixel sensor cell of claim 43, wherein said photoconversion device is coupled to said voltage source through said reset transistor and a transfer transistor which transfers accumulated charge from said photoconversion device (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80 and the transfer transistor).

35. Regarding claim 45, Compton discloses the pixel sensor cell of claim 41, wherein said pixel sensor cell is part of a CMOS imager (See Page 1, Section 0001 and Sections 0002 – 0005 to see how this limitation is met, It talks about image sensors having reset synchronized with mechanical shutter for controlling exposure).

36. Regarding claim 46, Compton discloses the pixel sensor cell of claim 41, wherein a reset voltage is readout after said shutter is closed (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a

result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

37. Regarding claim 47, Compton discloses the pixel sensor cell of claim 46, wherein a signal voltage is readout after said reset voltage is readout (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

38. Regarding claim 48, Compton discloses the pixel sensor cell of claim 41, wherein said pixel sensor cell comprises four transistors (See Figure 1).

39. Regarding claim 49, Compton discloses the pixel sensor cell of claim 41, wherein said readout circuitry reads out said charge through an output transistor and a row selection transistor (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select

transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

40. Regarding claim 51, Compton discloses a pixel sensor cell (Figure 3) comprising:

A photoconversion device for accumulating charge, said photoconversion device being coupled to and reset by a reset transistor to begin an integration period (Page 2, Section 0016 and 0019 See Figure 5A – 5D);

A mechanical shutter, wherein said mechanical shutter is open during the resetting of said photoconversion device and closed to end said integration period (Page 2, Section 0016 and 0019, See Figure 5A – 5D);

A charge collection region for receiving said charge from said photoconversion device (Page 2, Section 0015, the charge collection region or the floating region is reset by a reset gate 50 and receives charge from the photoconversion device); and

A readout circuit for reading out said charge from said charge collection region (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

41. Regarding claim 52, Compton discloses the pixel sensor cell of claim 51, wherein said photoconversion device is coupled to a voltage source (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

42. Regarding claim 53, Compton discloses the pixel sensor cell of claim 52, wherein said photoconversion device is coupled to a voltage source through a reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

43. Regarding claim 57, Compton discloses the pixel sensor cell of claim 51, wherein said readout circuitry reads out said charge through an output transistor and a row selection transistor (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

44. Regarding claim 59, Compton discloses the pixel sensor cell of claim 51, wherein said pixel sensor cell is part of a CMOS imager (See Page 1, Section 0001 and Sections 0002 – 0005 to see how this limitation is met, It talks about image sensors having reset synchronized with mechanical shutter for controlling exposure).

45. Regarding claim 60, Compton discloses a timing control circuit (Figure 3, Element 150) for an imager array comprising:

Circuitry (Figure 3, part of element 150) for applying driving voltage to at least one transistor of a pixel sensor cell of the array, wherein said transistor resets at least one photoconversion device to begin an integration period (Page 2, Section 0016 and 0019 See Figure 5A – 5D);

A mechanical shutter for ending said integration period (Page 2, Section 0016 and 0019, See Figure 5A – 5D); and

A readout circuit, wherein said readout circuit uses a rolling readout technique after said integration period ends (Page 2, Section 0015, The readout technique discussed in section 0015 is same as rolling readout, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

46. Regarding claim 61, Compton discloses the circuit of claim 60, wherein said pixel sensor cell further comprises a reset transistor for resetting a charge collection region and a transfer transistor for transferring charge to said charge collection region after said integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the

transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

47. Regarding claim 62, Compton discloses the circuit of claim 61, wherein said reset transistor and said transfer transistor are turned on simultaneously before said integration period to reset said photoconversion device (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

48. Regarding claim 63, Compton discloses the circuit of claim 60, wherein said photoconversion device is coupled to a voltage source (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

49. Regarding claim 64, Compton discloses the circuit of claim 63, wherein said photoconversion device is coupled to a voltage source through a reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

50. Regarding claim 66, Compton discloses the circuit of claim 64, wherein said photoconversion device is coupled to said voltage source through said reset transistor and a transfer transistor which transfers accumulated charge from said photoconversion device (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

51. Regarding claim 69, Compton discloses the circuit of claim 64, wherein said photoconversion device is coupled to said voltage source directly by one of said at least two reset transistors (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

52. Regarding claim 70, Compton discloses the circuit of claim 60, wherein said rolling readout is conducted by reading out successive rows of said imager array (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

53. Regarding claim 71, Compton discloses the circuit of claim 60, wherein said imager array is part of a CMOS imager (See Page 1, Section 0001 and Sections 0002 – 0005 to see how this limitation is met, It talks about image sensors having reset synchronized with mechanical shutter for controlling exposure).

54. Regarding claim 72, Compton discloses a processor system (Figure 3) comprising:

A processor (Figure 3, Element 150); and

An imager (Figure 3, Element Image sensor) coupled to said processor, said imager comprising:

A timing control circuit (Figure 3, Element 150, Processor works at timing control circuit) for globally resetting pixel sensor cells of said imager before an integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20),

A mechanical shutter (Figure 3, Element 160) for ending said integration period (Page 2, Section 0016 and 0019, and 0020, See Figure 5A – 5D), and

A readout circuit (Figure 3, Element 150), wherein said readout circuit uses a rolling readout technique after said integration period ends (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

55. Regarding claim 73, Compton discloses the system of claim 72, wherein said pixel sensor cell comprises a reset transistor for resetting said charge collection region and a transfer transistor for transferring charge to said charge collection region after said integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the

transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

56. Regarding claim 74, Compton discloses the system of claim 73, wherein said reset transistor and said transfer transistor are turned on simultaneously before said integration period to reset said photoconversion device (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

57. Regarding claim 75, Compton discloses the system of claim 72, wherein said photoconversion device is coupled to a voltage source (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

58. Regarding claim 76, Compton discloses the system of claim 75, wherein said photoconversion device is coupled to a voltage source through a reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

59. Regarding claim 78, Compton discloses the system of claim 76, wherein said photoconversion device is coupled to said voltage source through said reset transistor and a transfer transistor which transfers accumulated charge from said photoconversion device (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

60. Regarding claim 82, Compton discloses the system of claim 72, wherein said rolling readout is conducted by reading out successive rows of said imager array (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

61. Regarding claim 83, Compton discloses the system of claim 72, wherein said imager array is part of a CMOS imager (See Page 1, Section 0001 and Sections 0002 – 0005 to see how this limitation is met, It talks about image sensors having reset synchronized with mechanical shutter for controlling exposure).

62. Regarding claim 84, Compton discloses an imager device (Figure 3 and 2) comprising:

A pixel array (Figure 2) comprising:

A plurality of pixels (Figure 2, Element 10);

Readout circuitry (Figure 3, Element 150) for said array (Page 2, Section 0015, The readout technique discussed in section 0015 is same as rolling readout, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row

select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).;

Global circuitry (Figure 1, Element 150) for resetting photoconversion devices of said array to begin an integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20) ; and

A mechanical shutter for ending said integration period (Page 2, Section 0016 and 0019, and 0020, See Figure 5A – 5D).

63. Regarding claim 85, Compton discloses the device of claim 84, wherein said pixels are readout on a row by row basis after the mechanical shutter is closed and the first integration period ends (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

64. Regarding claim 86, Compton discloses the device of claim 84, wherein said global reset is conducted by turning on a reset transistor and a transfer transistor within each pixel to couple the photoconversion device of each pixel to a voltage source (Page

2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

65. Regarding claim 87, Compton discloses the device of claim 86, wherein said reset transistor and said transfer transistor are turned on simultaneously to begin said integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

66. Regarding claim 88, Compton discloses the device of claim 84, wherein said readout circuitry comprises circuitry for reading out reset voltages and output voltages for said plurality of pixels (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

67. Regarding claim 89, Compton discloses the device of claim 84, wherein said global circuitry for resetting said photoconversion devices comprises circuitry for coupling said photoconversion device to a voltage source (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40

to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

68. Regarding claim 90, Compton discloses the device of claim 89, wherein said photoconversion device is coupled to a voltage source through a reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

69. Regarding claim 92, Compton discloses the device of claim 90, wherein said photoconversion device is coupled to said voltage source through said reset transistor and a transfer transistor which transfers accumulated charge from said photoconversion device (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80 and the transfer gate).

70. Regarding claim 93, Compton discloses An imager integrated circuit (Figure 1 and 2) comprising:

A doped layer formed in a substrate (It Is known in the art);

An array of pixel sensor cells formed in said doped layer, wherein said pixel sensor cells are globally reset before an integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20); and

Signal processing circuitry (Figure 3, Element 150) formed in said substrate and

electrically connected to the array for receiving and processing pixel signals representing an image acquired by the array and for providing output data representing said image (Page 2, Section 0015).

71. Regarding claim 94, Compton discloses the imager integrated circuit of claim 93, wherein said pixel sensor cell further comprises a reset transistor for resetting a charge collection region and a transfer transistor for transferring charge to said charge collection region after said integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

72. Regarding claim 95, Compton discloses the imager integrated circuit of claim 94, wherein said reset transistor and said transfer transistor are turned on simultaneously before said integration period to reset said photoconversion device (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

73. Regarding claim 96, Compton discloses the imager integrated circuit of claim 94, wherein said photoconversion device is coupled to a voltage source (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

74. Regarding claim 97, Compton discloses the imager integrated circuit of claim 96, wherein said photoconversion device is coupled to a voltage source through a reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

75. Regarding claim 99, Compton discloses the imager integrated circuit of claim 97, wherein said photoconversion device is coupled to said voltage source through said reset transistor and a transfer transistor which transfers accumulated charge from said photoconversion device (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

76. Regarding claim 103, Compton discloses the imager integrated circuit of claim 93, wherein said signal circuitry further comprises readout circuitry for reading out said signals (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

77. Regarding claim 104, Compton discloses the imager integrated circuit of claim 103, wherein said readout circuitry reads out said signals using a rolling readout (Page

2, Section 0015, The readout technique discussed in section 0015 is same as rolling readout, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

78. Regarding claim 105, Compton discloses the imager integrated circuit of claim 93, wherein said rolling readout is conducted by reading out successive rows of said imager array (Page 2, Section 0015, The readout technique discussed in section 0015 is same as rolling readout, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

79. Regarding claim 106, Compton discloses the imager integrated circuit of claim 93, wherein said imager is a CMOS imager (See Page 1, Section 0001 and Sections 0002 – 0005 to see how this limitation is met, It talks about image sensors having reset synchronized with mechanical shutter for controlling exposure).

Claim Rejections - 35 USC § 103

80. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

81. Claims 10, 17 – 23, 27 – 30, 50, and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Compton (US 2004/0081446 A1) in view of Yadid-Pecht et al. (US 6,515,702 B1).

82. Regarding claim 10, Compton teaches reading out charges

Compton failed to teach charges are sampled by a sample/hold circuit after said readout.

Yadid-Pecht teaches a CMOS imaging device comprising a sample and hold circuitry for storing and sampling a charges outputted or readout from a readout circuit. (Col 3, Line 33 – 49)

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the CMOS imaging device of Compton with a sample/Hold circuitry for storing and sampling charges outputted or readout from a readout circuit. As taught in Yadid-Pecht. The motivation to do so is that sample and hold circuits are used to hold the analogue value steady for a short time while the

converters or other systems of imaging device performs some operation that takes a little time.

83. Regarding claim 17, Compton disclose a method of operating a pixel of an image sensor comprising:

Opening a mechanical shutter (Page 2, Section 0016 and 0019, See Figure 5A – 5D);

Resetting a photoconversion device after said mechanical shutter is opened to begin a first integration period (Page 2, Section 0016 and 0019 See Figure 5A – 5D);

Accumulating charge in said photoconversion device during said first integration period (Page 2, Section 0015);

Resetting a charge collection region by operating a gate of a reset transistor to obtain a reset voltage (Page 2, Section 0015, the charge collection region or the floating region is reset by a reset gate 50);

Reading out said reset voltage at said charge collection region by operating a gate of a row select transistor (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing) ;

Transferring said charge from said photoconversion device to said charge collection region by operating a gate of a transfer transistor (Page 2, Section 0015 and

0016); and

Reading out the charge residing in said charge collection region to obtain a pixel signal voltage (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing); and

Compton failed to teach charges (Readout reset voltage and Pixel Signal voltage) are sampled by a sample/hold circuit after said readout.

Yadid-Pecht teaches a CMOS imaging device comprising a sample and hold circuitry for storing and sampling a charges (Readout reset voltage and Pixel Signal voltage) are outputted or readout from a readout circuit. (Page 3, Section 0034, and Page 4, Section 0048)

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the CMOS imaging device of Compton with a sample/Hold circuitry for storing and sampling charges (Readout reset voltage and Pixel Signal voltage) are outputted or readout from a readout circuit as taught by Yadid-Pecht. The motivation to do so is that sample and hold circuits are used to hold the analogue value steady for a short time while the converters or other systems of imaging device performs some operation that takes a little time.

Regarding claim 18, Yadid-Pecht disclose the method of claim 17, further comprising

producing a differential signal for each pixel which comprises the difference between the sampled reset voltage and the sampled pixel signal voltage (Page 3, Section 0034, and Page 4, Section 0048)

.

Regarding claim 19, Compton discloses the method of claim 17, wherein said act of reading out the reset voltage comprises reading out the reset voltage from the charge collection region (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

Regarding claim 20, Compton discloses the method of claim 17, wherein said photoconversion device resetting comprises turning on said reset transistor and said transfer transistor before said integration period (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

Regarding claim 21, Compton disclosesthe method of claim 20, wherein said reset transistor and said transfer transistor are turned on simultaneously (Page 2, Section

0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

Regarding claim 22, Compton discloses the method of claim 17, wherein said photoconversion resetting comprises coupling said photoconversion device to a voltage source (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

Regarding claim 23, Compton discloses the method of claim 22, wherein said photoconversion device is coupled to a voltage source through a reset transistor (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

Regarding claim 27, Compton discloses the method of claim 22 wherein said photoconversion device is coupled to said voltage source through said reset transistor and a transfer transistor which transfers accumulated charge from said photoconversion device (See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

Regarding claim 28, Compton discloses the method of claim 17, wherein said image sensor is a CMOS image sensor (See Page 1, Section 0001 and Sections 0002 – 0005 to see how this limitation is met, It talks about image sensors having reset synchronized with mechanical shutter for controlling exposure).

Regarding claim 29, Compton discloses the method of claim 17, wherein said charge collection region is a floating diffusion region (Page 1, Section 0015, and the charge collection region is Floating Diffusion 40).

Regarding claim 30, Compton discloses the method of claim 17, wherein said act of reading out charge further comprises reading out said charge through an output transistor and a row selection transistor (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing).

Regarding claim 50, Compton teaches reading out charges.

Compton failed to teach charges are sampled by a sample/hold circuit after said readout.

Yadid-Pecht teaches a CMOS imaging device comprising a sample and hold circuitry for storing and sampling a charges outputted or readout from a readout circuit. (Page 3, Section 0034, and Page 4, Section 0048)

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the CMOS imaging device of Compton with a

sample/Hold circuitry for storing and sampling charges outputted or readout from a readout circuit as taught in Yadid-Pecht. The motivation to do so is that sample and hold circuits are used to hold the analogue value steady for a short time while the converters or other systems of imaging device performs some operation that takes a little time.

Regarding claim 58, Compton teaches reading out charges.

Compton failed to teach charges are sampled by a sample/hold circuit after said readout.

Yadid-Pecht teaches a CMOS imaging device comprising a sample and hold circuitry for storing and sampling a charges outputted or readout from a readout circuit. (Page 3, Section 0034, and Page 4, Section 0048)

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the CMOS imaging device of Compton with a sample/Hold circuitry for storing and sampling charges outputted or readout from a readout circuit as taught in Yadid-Pecht. The motivation to do so is that sample and hold circuits are used to hold the analogue value steady for a short time while the converters or other systems of imaging device performs some operation that takes a little time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELAM T. GEBRIEL whose telephone number is (571)270-1652. the examiner can normally be reached on Monday-Thursday 7.30am-

5.00pm.If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu NgocYen can be reached on 571-272-7320. the fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Monday, October 13, 2008

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